SPECIFICATION AMENDMENTS

Please replace paragraph 4 with the following rewritten paragraph:

In more recent practices, the laser ablation method is preferred ~~used~~ since it is faster, more accurate and leaves less residue within the fuse link window area. However, as device sizes decrease to 0.25 microns and multi-level device circuitry is employed to achieve the desired circuit density, Low-K (low dielectric constant) materials have become necessary in the formation of dielectric insulating layers, also referred to as inter-metal dielectric (IMD) layers in order to reduce circuit capacitance and therefore increase signal transport speeds. Low-K materials may include porous inorganic silicon oxide based materials which are generally less mechanically strong and subject to cracking when subjected to thermal mismatch stresses.

Please replace paragraph 6 with the following rewritten paragraph:

Generally fuse link structure have been limited to metals

with a low melting point, such as aluminum since less energy is required to destroy the fuses, and sufficient energy can easily be transported through overlying light transparent windows. While the use of copper would be desirable in that the same process technology could be used for forming the fuse link structure as is used for forming metal interconnects in underlying layers, such as damascenes, ~~copper,~~ the use of copper damascene fuse links has presented several problems in implementation.

Please replace paragraph 7 with the following rewritten paragraph:

For example, copper generally requires much higher levels of energy to destroy a copper fuse, due to its high thermal conductivity and it higher melting point compared to aluminum. In addition, the fuse link layer, also referred to as a redundancy layer, is typically a thicker layer for various reasons with the metal fuses having thicknesses of about 10,000 Angstroms. The use of high laser energies or electrical current energies required to destroy a copper fuse frequently causes damage to underlying dielectric insulating layers, for example low-K dielectric insulating layers, thereby reducing [[a]] wafer

yield and device reliability.

Please replace paragraph 17 with the following rewritten paragraph:

It will additionally be appreciated that the metallization levels including interconnecting vias may be formed by single or dual damascene processes where the metallization layers may include different metals or conductive material in each metallization layer. For example, the guard ring structure surrounding the fuse link area and the fuse interconnect structures may be formed of any metal including alloys of copper, tungsten, and aluminum as well as including etch stop layers such as metal nitrides, metal oxynitrides, metal carbides and metal oxycarbides between IMD layer portions and barrier/adhesive layers lining the filled metal damascenes. The guard ring structure is preferably included to surround the fuse link circuitry extending through at least about three metallization levels to prevent crack propagation and residual metal diffusion following ~~the~~ a fuse blowing operation. The guard ring structure is electrically isolated, formed of dummy metal interconnect portions.